METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING A LOW K DIELECTRIC

Related Application

This invention is related to a U.S. Patent Application having docket number SC12765TP, filed September 11, 2003, entitled, "Integration of Ultra Low K Dielectric in a Semiconductor Fabrication Process," and assigned to the assignee hereof.

Field of the Invention

The present invention is in the field of semiconductor devices and more particularly in the field of semiconductor fabrication processes employing low K dielectrics.

Related Art

In the field of semiconductor fabrication, the use of dielectric materials having a low dielectric constant (low K materials) is well known. Low K dielectrics are used primarily in backend processing. Backend processing refers generally to processing subsequent to the formation of transistors in the wafer substrate to connect the transistors (typically with multiple levels of interconnects). Each interconnect level is separated by an interlevel dielectric (ILD). The individual interconnects within a single interconnect level are also separated by a dielectric material that may or may not be the same as the ILD. Vias or contacts are formed in the ILD's and filled with conductive material to connect the interconnect levels in a desired pattern to achieve a desired functionality.

The spacing between adjacent interconnects within an interconnect level and the spacing between vertically adjacent levels have both decreased as device complexity and performance have increased. Minimizing cross coupling between the many signals within a device is now a significant design consideration. The primary source of signal cross coupling or cross talk is capacitive. A pair of adjacent interconnect (whether within a single interconnect level or in vertically adjacent interconnect levels) separated by an intermediate dielectric material form an unintended parallel plate capacitor. Minimizing cross coupling requires a minimization of the capacitance between any pair of adjacent interconnects, especially those interconnects that carry signals that switch at high frequency.

One popular approach to minimizing cross talk includes the use of low K dielectric materials as the interconnect dielectric. Low K materials reduce cross talk because the capacitance of a parallel plate capacitor is directly proportional to the dielectric constant of the material between the capacitor plates. A lower dielectric constant material translates into lower capacitance and lower cross coupling.

Various low K materials have been used in low K backend processing with mixed results. Integration of low K material into existing fabrication processes is particularly challenging in the case of backend processing that includes the use of chemical mechanical polishing (CMP). CMP is a technique by which each interconnect level is formed in many existing processes. In a CMP process, as implied by its name, a film or layer is physically polished with a rotating polishing pad in the presence of a "slurry" that contains mechanical abrasion components and/or chemical components to produce a smooth upper surface and to remove excess conductive material and thereby isolate the individual interconnects from one another.

Low K materials are generally not easily integrated into a CMP-based backend process. Low K materials tend to exhibit dishing and erosion and other forms of deterioration under chemical mechanical polishing and are susceptible to slurry penetration into the Low K material. To combat this problem, capping materials have been formed over the low K dielectrics to act as a CMP stop. Unfortunately, adhesion between many materials used as low K materials and other materials suitable for use as a CMP stopping layer is often not good. TEOS, for example, is a good CMP stopping layer, but it doesn't adhere well to typical low K dielectrics. It would be desirable, therefore, to implement a process integrating low K interconnect dielectrics into a CMP backend process flow.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limited by the accompanying figures, in which like references indicate similar elements, and in which:

FIG. 1 is a cross section of a semiconductor device at a stage in processing according to an embodiment of the invention;

FIG. 2 is a cross section of the semiconductor device of FIG. 1 at a subsequent stage in processing according to the embodiment of the invention;

FIG. 3 is a cross section of the semiconductor device of FIG. 2 at a subsequent stage in processing according to the embodiment of the invention;

FIG. 4 is a cross section of the semiconductor device of FIG. 3 at a subsequent stage in processing according to the embodiment of the invention;

FIG. 5 is a cross section of the semiconductor device of FIG. 4 at a subsequent stage in processing according to the embodiment of the invention; and

FIG. 6 is a cross section of the semiconductor device of FIG. 5 at a subsequent stage in processing according to the embodiment of the invention.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

Detailed Description of the Drawings

In one aspect, a low K dielectric layer and a cap for the low K dielectric layer are formed in situ using the same silicon precursors but at different precursor ratios. The low K dielectric is deposited with precursors that are useful for making a low K dielectric. Trenches are formed in the low K dielectric and are filled by a metal layer. Chemical mechanical processing (CMP) is utilized to remove the metal outside the trench while the cap aids planarity outside the trench. This is better understood by reference to the drawings and the following specification.

Shown in FIG. 1 is a semiconductor device 10 comprising a substrate 12, a dielectric 14 over substrate 12, a metal line 16 in dielectric layer 14 at the surface of dielectric layer 14, and dielectric layer 18. Metal line 16 is shown separated from substrate 12 by only dielectric 14 but other structures not shown for ease of understanding may also be present. Similarly dielectric layer 14 may also be a composite of a variety of dielectric layers. Dielectric layer 18 is a carbon-doped silicon oxide that is deposited in a plasma CVD chamber to a thickness of about 5000 Angstroms by introducing octamethylcyclotetrasiloxane (OMCTS), oxygen, ethylene, and helium at a temperature of about 400 degrees Celsius, a pressure of about 7 Torr, and a power of about 900 watts. The flow ratio of OMCTS to oxygen is about 8 milligrams per minute to 1 standard cubic centimeter (SCCM). The flow rate of OMCTS is about 5000 milligrams per minute. The nominal dielectric constant is about 2.6 but should not be greater than about 2.7. A dielectric constant of less than 3.0, which is a desirable achievement for a low k dielectric, is thus obtained. The ratio of the milligrams per minute of the OMCTS to the SCCM of the oxygen should be at least two to one. Also other temperatures, pressures, powers and thicknesses can be effective. For example, temperature can be 250

to 450 degrees Celsius. The pressure can be 4 to 10 Torr. The power can be 500 to 1000 watts. The flow rate of the OMCTS 2000 and 8000 milligrams per minute. The thickness can be between 2000 to 8000 Angstroms. Other parameters than the ranges listed above may also be effective. The helium acts as a carrier gas for the OMCTS and is applied at about 1000 SCCM. This can vary greatly. The ethylene, which has a flow rate of about 2000 SCCM, acts as a reaction buffer to limit the reaction of the OMCTS and the oxygen at the film surface as it is being formed. This flow rate can also vary greatly.

Shown in FIG. 2 is semiconductor device after deposition of a cap 20 that is formed in situ with low K dielectric layer 18. Cap 20 is deposited by changing the ratio of the milligrams of OMCTS to the SCCM of oxygen to about 1 to 2.5. This should be not greater than about 1 to 1. The pressure is reduced to about 3 Torr. This can vary from 1 to 10. Otherwise, the parameters are left the same. The pressure is preferably reduced to increase ion bombardment on the film, cap 20, as it is being deposited to increase its density. The parameters may also be changed for this. The primary desired effect is achieved from the ratio of the flow rates of OMCTS to oxygen being reduced to form cap 20 with the desired characteristics. Cap 20, formed in this way, has characteristics beneficial for protecting an underlying low K dielectric during the CMP process. The thickness of cap 20 is about 1500 Angstroms so that a total of about 6500 Angstroms for cap 20 and low K dielectric 18. Cap 20 may also be another thickness, for example between 500 to 2000 Angstroms.

Cap 20 so formed is effective as a layer that protects an underlying low K dielectric that is relatively soft and subject to dishing. Cap 20 is significantly harder than underlying low K dielectric layer 18 and has been found to be useful for subsequent protection for dielectric layer 18 under CMP processing. This processing results in a carbon concentration that is quite small but

measurably greater than some oxide films. For example the oxygen to carbon ratio is about 3600 to 1, whereas it is about 20,000 to 1 for TEOS oxide. Similarly the ratio of silicon to carbon is about 85 to 1, whereas it is about 350 to 1 for TEOS. The silicon to carbon ratio should be less than about 175 to 1. These intensity ratios are based on measurements using the time of flight secondary ion mass spectroscopy technique.

Shown in FIG. 3 is semiconductor device 10 after forming a trench 22 and a trench 24 in cap 20 and low K dielectric 18. Trench 22 is over metal line 16. Trenches 22 and 24 are about 4500 Angstroms deep. The process for forming trenches is known to one of ordinary skill in the art.

Shown in FIG. 4 is semiconductor device 10 after formation of a via hole 26 in dielectric 18 between metal line 16 and the bottom of trench 22. Via hole 26 is about 2000 Angstroms deep. The process for forming vias from a trench, whether before or after forming the trench, is known to one of ordinary skill in the art.

Shown in FIG. 5 is semiconductor device 10 after deposition of a metal layer 28 that fills via hole 26 and trenches 22 and 24 as well as extending over cap 20. Typical metals used for this purpose include aluminum and copper. In both cases there is generally a barrier layer included as well. In any event, deposition of metal to fill trenches and overlie the surrounding dielectric is known to one of ordinary skill in the art.

Shown in FIG. 6 is semiconductor device 10 after a CMP process step which removes metal layer 28 that is on cap 20. The CMP process also removes at least a portion of cap 20. This leaves metal portions 30 and 32 from metal layer 28 in trenches 22 and 24. Metal portion 30 is also in via hole 26 that completes the via to metal line 16. It is beneficial to remove at least a portion of cap 20 because it is a higher K than low K dielectric layer 18. The

result is that the surface of the metal in trenches 22 and 24 and the surface of cap 20 are substantially coplanar. Metal line 16, along with metals 30 and 32 form a useful interconnect for semiconductor device 10. Removing metal by CMP to leave a substantially planar surface is known to one of ordinary skill in the art.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. For example, OMCTS has been described as a useful the dominant precursor but another dominant precursor could also be used. For example tetramethylcyclotetrsiloxanes (TMCTS) may be used instead of OMCTS. Also, metal has been described as filling the trenches followed by CMP. There may, however, be situations in which CMP is required on other structures such as a via level, with another fill material, or even no fill material for the case of a trench as a wave guide. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not

include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.